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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,489	04/12/2004	Hongjian Gan	JCLA12709	4944

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EXAMINER	
RUTLAND WALLIS, MICHAEL	
ART UNIT	**PAPER NUMBER**
2835	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,489	GAN ET AL.	
	Examiner	Art Unit	
	Michael Rutland-Wallis	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 10-13, 15, 16-18, 19, 20, 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Pat. No. 6,771,052) in view of Giannopoulos et al. (U.S. Pat. No. 6,549,432)

With respect to claims 1, 11, 15, 18, 19 and 22 Ostojic teaches a power supply (item 100) with multiple outputs (see Fig. 2, items 116 and 132), comprising: a front-end converter (item 102) with a current mode output (item 104); a first buck converter (item 108 see Fig. 2) and a second buck converter (item 108 see Fig. 2). Ostojic also teaches a time delay synchronous control circuit (controller item 120 see col. 7 line 47-58 for description of synchronous or alternate control), for controlling the time of switching the buck converters. Ostojic does not teach the connection of a capacitor connected with the front-end converter or the control of a time delay between the front-end converter. Giannopoulos teaches the connection of a similar controller (item 530) to sequentially control the output voltage circuits and input voltage pulse from a front-end converter (item 502), wherein the output capacitor (see capacitor Fig. 5 labeled Vin connected

across item 502 and S0 to control pulse from the front-end converter), which is cascaded, to output to both converters. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of a first output capacitor and controller seen in Giannopoulos to synchronously control the time delay between the front-end converter and a pulse supplied to a first and second converter arrangement in order to provide a soft switching and input switch (Giannopoulos col. 2 lines 30-35) control the time period and voltage and current level supplied to converters.

With respect to claim 10 Giannopoulos teaches an anode of the first rectifier diode (D2) is connected to a nominal terminal of a first secondary winding of the transformer (ns) and an anode of the second rectifier diode (D2) is connected to a reverse terminal of a second secondary winding of the transformer, a connection terminal of the first and second secondary windings is connected to the output as the ground of a secondary side of the transformer (Fig. 5 and 7).

With respect to claim 12 Ostojic as modified by Giannopoulos teach the buck switches of both the first and second buck converters are turned off before the pulse output current of the front-end converter reaches to zero (see timing diagram Fig. 6 in Giannopoulos).

With respect to claims 13 and 20 Ostojic as modified by Giannopoulos the delay time behind the time when the front-end converter begins to have the pulse output current, the first buck converter is turned on and then the first buck converter is turned off, at the time the first buck converter being turned off, the second buck converter is sequentially turned on see (see timing diagram Fig. 6 in Giannopoulos).

With respect to claim 16 Giannopoulos teaches a delay time (Ton0) exists between the time the front-end converter begins to have the pulse output current and the time the first buck converter or the second buck converter are turned on (Ton 2).

With respect to claim 17 Ostojic as modified by Giannopoulos teaches both of the first and second buck converters are turned off before the pulse output current of the front-end converter reaches to zero (see timing diagram Fig. 6 in Giannopoulos).

With respect to claim 23 Ostojic as modified by Giannopoulos teach the converter is a flyback converter.

With respect to claim 24 Ostojic as modified by Giannopoulos teach the rectifier is a diode rectifier or a synchronous rectifier.

Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Pat. No. 6,771,052) in view of Giannopoulos et al. (U.S. Pat. No. 6,549,432) in further view of Huang et al. (U.S. Pat. No. 6,344,979)

With respect to claim 2 Ostojic as modified by Giannopoulos do not teach the converter is a LLC-SRC as described, Huang teaches such a converter It would have been obvious to one of ordinary skill in the art at the time of the invention to utilize such a converter in order to power conversion efficiency and switching.

With respect to claims 3 and 4 Ostojic is silent on the internal circuitry of the front-end converter. Giannopoulos teaches the front-end converter comprising: a bridge circuit including (bridge rectifier) a pair of power switches (diodes), the bridge circuit being coupled to an input voltage; a resonant tank (formed with capacitor and transformer seen in Fig. 5), further Huang teaches a switching converter and resonant

tank. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of a additional circuitry of a tank circuit and control as such circuitry in order to output a clear power signal as such circuitry is typical in such converters.

With respect to claim 5 and 6 Huang teaches the resonant tank comprising: a series resonant capacitor (Cs), coupled to the bridge circuit (S1 and S2 or see Giannopoulos); a series resonant inductor (Ls), coupled to the series resonant capacitor; and a transformer (item 130) with a magnetizing inductor coupled to the series resonant inductor and the bridge circuit, wherein the series resonant capacitor, the series resonant inductor and the magnetizing inductor constitute two characteristic frequencies of the resonant tank.

With respect to claim 7 Giannopoulos teaches the bridge circuit comprises a bus capacitor (Fig. 5) coupled to the input voltage.

With respect to claim 8 Ostojic and Huang teach the transformer comprising a primary winding and two secondary windings connected in series in phase, for isolating the bridge circuit and the resonant tank from the rectifier.

With respect to claim 9 Giannopoulos teaches the rectifier is a full-wave rectifier comprising a first rectifier diode and a second rectifier diode connected to the output capacitor, the first and second rectifier diodes are connected through the output capacitor to an output filter to generate an output voltage of the multiple outputs of the power supply.

Claims 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ostojic (U.S. Pat. No. 6,771,052) in view of Giannopoulos et al. (U.S. Pat. No. 6,549,432) in further view of Crane (U.S. Pat. No. 5,400,239)

With respect to claim 14 and 21 Ostojic as modified by Giannopoulos teach the alternate and sequentially switching of the first and second converter and no overlap existing. Ostojic as modified by Giannopoulos does not teach the internal switching scheme where a dead conduction time exits every two of the output current pulses of the front-end converter and second converter. Crane teaches such a switching scheme (item 50). It would have been obvious to one of ordinary skill in the art at the time of the invention to use such an alternate switching scheme in order to provide a timing sequence to control output multiple voltages.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bourdillon (U.S. Pat. No. 6,552,917) teaches a similar device disclosed in Applicant's claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Rutland-Wallis whose telephone number is 571-272-5921. The examiner can normally be reached on Monday-Thursday 7:30AM-6:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn D. Feild can be reached on 571-272-2092. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MRW

ANATOLY VORTMAN
PRIMARY EXAMINER